REMARKS/ARGUMENTS

The applicants' attorneys appreciate the Examiner's thorough search and remarks.

Responsive to the objection set forth in paragraph 1 of the Office Action, the title has been amended. Withdrawal of the objection is requested.

It is acknowledged with appreciation that claim 3 is deemed allowable if rewritten in independent form. Accordingly, claim 3 has been amended to include the limitations of its base claims. Confirmation of the allowability of claim 3 is requested.

Claim 1 has been rejected as anticipated by Tsui, U.S. Patent No. 6,489,204. Reconsideration is requested.

A process according to the present invention calls for forming a termination trench, and oxidizing the termination trench prior to forming the gate trenches. Thus, as seen in Figures 2a-2c, a hard mask formed from an oxidation retardant material (e.g. silicon nitride) is etched to expose a portion of the silicon body in which the termination trench is formed, then the termination trench is formed. Thereafter, field oxide is formed over the sidewall and the bottom of the termination trench. After the field oxide formation, the gate trenches are formed.

An important characteristic of a power device is its ability to carry current. The ability to carry current can be increased by increasing cell density. One way to increase cell density in a trench type device is to reduce the trench width. When a trench termination is formed and covered with field oxide prior to forming gate trenches, as is the case with the present invention, the width of the gate trenches can be reduced. Specifically, as explained in the specification, because

> the field oxide is below the top surface of the die, wafer planarity at active trench lithography stage is improved greatly. The much improved wafer surface planarity at trench lithography stage allows for further reduction of trench width by as much as 20%. This reduction in size makes it possible to, for example, increase the density of the trenches thus increasing channel density while keeping the gate charge low, especially the Q_{GD} and Q_{SWITCH}.

See specification, page 2, paragraph 6.

Thus, claim 1 now calls for

1. A method for manufacturing a semiconductor device comprising:

providing a semiconductor die of a semiconductive material having a channel receiving layer of a first conductivity;

forming a layer of oxidation retardant material over said channel receiving layer;

removing a portion of said oxidation retardant material to expose said semiconductor die;

etching said exposed semiconductor die to form a termination recess around said oxidation retardant material remaining after said receiving step, said termination recess including a sidewall and a bottom;

forming an oxide on said sidewall and said bottom of said termination recess; and

forming trenches in said channel receiving layer after forming said oxide on said sidewall and said bottom of said termination recess.

Each of claims 2 and 13-15 depends from claim 1 and, therefore, includes its limitations. Each of these claims includes other limitations, which in combination with those of claim 1 are not shown or suggested by the art of record.

Claim 16 has been rejected as anticipated by Tsui. Claim 16 has been amended, and now calls for "forming a low temperature oxide body over all of said gate structure and at least a portion of said conductive region, and forming recesses on a top portion of said low temperature oxide body". These features are not shown or suggested by Tsui. Claim 16 should, therefore, be deemed allowable. Reconsideration is requested.

Each of claims 17-20 includes the limitations of claim 16 as it depends from the same. Each of these claims includes other limitations, which in combination with those of claim 16 are not shown or suggested by the art of record. Reconsideration is requested.

The application is believed to be in condition for allowance. Such action is earnestly solicited.

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on November 16, 2004:

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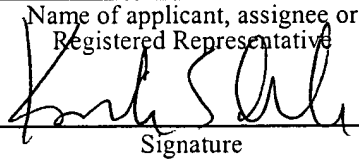
Name of applicant, assignee or Registered Representative



Signature

November 16, 2004

Date of Signature

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Respectfully submitted,

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